Variational Capacitance Extraction of On-Chip Interconnects Based on Continuous Surface Model

Wenjian Yu[1,3],   Chao Hu[2,3],   Wangyang Zhang[1,3]

[1]Department of Computer Science and Technology, [2]Institute of Microelectronics, [3]Tsinghua National Laboratory for Information Science and Technology, Tsinghua University, Beijing 100084, China
E-mail: yu-wj@tsinghua.edu.cn, huc07@mails.tsinghua.edu.cn, zwy677@gmail.com

ABSTRACT

In this paper we present a continuous surface model to describe the interconnect geometric variation, which improves the currently used model for better accuracy while not increasing the number of variables. Based on it, efficient techniques are presented for chip-level capacitance extraction considering the window technique. The sparse-grid-based Hermite polynomial chaos combined with a novel weighted principle factor analysis is employed for intra-window extraction. Then, the inter-window capacitance covariance is calculated through matrix pseudo inverse. Numerical results validate the accuracy and efficiency of the proposed method, which is more than 50 times faster than the Monte-Carlo simulation with 10000 samples.

Categories and Subject Descriptors

J.6 [COMPUTER-AIDED ENGINEERING]: Computer-aided design (CAD); I.6 [Computing Methodologies]: Simulation and Modeling

General Terms

Algorithms, Theory, Design

Keywords

Geometric variation modeling, Hermite polynomial chaos method, quadratic variation model, spatial correlation, variational capacitance extraction

1. INTRODUCTION

As technology scales down to the nanometer era, the parasitic capacitance is delivering more impact on performance of integrated circuits. Delay caused by interconnect parasitics has already overtaken gate delay to become the major limiting factor of performance. At the same time, the increased mismatch between the actual fabricated interconnects and those in design brings great challenges to the computational accuracy and efficiency of parasitic capacitance extraction.

Process variations can be classified into systematic variations and random variations [1]. The systematic variations are often pattern-dependent and can be modeled with some deterministic methods [2]. In contrast, the nature of random variations is more complicated and a stochastic modeling methodology is needed for capacitance extraction. The random variation is mainly due to process uncertainty and results in non-smooth geometry surfaces

of both conductor and dielectric. Another important character of on-chip variation is the spatial correlation. Thus, a spatially correlated multivariate Gaussian distribution is often assumed for the geometry parameter variations [3-9].

A straight-forward approach for variation-aware capacitance extraction is the Monte Carlo method, which suffers from huge computing time with thousands of stochastic samplings. Although it can be accelerated with the quasi-Monte-Carlo techniques [10], the latter only generates the mean and standard deviation of capacitance, which is often not sufficient as an accurate model required by the subsequent statistical circuit analysis. A non-Monte-Carlo method was firstly proposed for variation-aware capacitance extraction [3-4], which emphasizes on the off-chip rough surface effect. The technique can only compute the mean and standard deviation of capacitance, but an accurate high-order variation model. Based on a 3-D boundary element method (BEM) capacitance solver, a perturbation method was proposed in [5] to generate a quadratic model for capacitance variation. Two efficient methods were then proposed to obtain the quadratic variational capacitance with the Hermite polynomial chaos [6, 7]. The spectral stochastic collocation method (SSCM) in [6] employs the techniques of homogenous chaos expansion and sparse grid quadrature to obtain the coefficients in the quadratic expression. The method in [7] employs the spectral stochastic method, and then solves augmented potential coefficient matrices. Considering only the first-order variation of potential coefficients, this method is very efficient, but not promising on the accuracy. Recently, a method combining the Neumann expansion and Hermite expansion was proposed for impedance extraction [8]. The computational efficiency is greatly improved for rough-surface structures with a large number of random variables.

Although the methods in [5-7] generate quadratic variation model of capacitance, which has merit for subsequent statistical circuit analysis, they all consider a simplified model of geometric variations. The variational geometry is constructed by disturbing the panels on nominal conductor surface, which produces an incomplete surface. This surface discontinuity obviously deviates from the actual situation, and is likely to induce large error for the interconnect capacitance under nanometer technology process. Another shortage of [5-7] is that they do not consider the actual chip-level capacitance extraction. Recently, techniques considering the window-based chip-level capacitance extraction were proposed in [9]. A so-called Hermite polynomial collocation (HPC) method is employed to extract the intra-window interconnects. And then, the capacitance covariances between windows and the statistical full-path capacitance are calculated. However, [9] uses an even simpler grid-based variation model than [5-7], to avoid the difficulty of random variable reduction.

In this paper, the variation-aware capacitance extraction for on-

chip interconnects is considered, where the correlation length of variables are not as short as that in the rough-surface structures. We firstly present a new geometric variation model, which generates continuous surface while not increasing the number of variables. Experimental results are also presented to reveal the inaccuracy of capacitance caused by the simple geometric model in [5-7]. Based on the variation model with continuous surfaces, the techniques in [9] are extended for chip-level window-based capacitance extraction. A weighted principle factor analysis (wPFA) technique is proposed to reduce the random variables while considering their different contributions to the resulting capacitance. The pseudo inverse of matrix is utilized to derive the capacitance covariance between windows. With these techniques, both variational intra-window capacitances and full-path capacitance cross windows can be computed efficiently. Numerical results show that the proposed method is about 50 times faster than the Monte-Carlo method, while preserving high accuracy.

2. BACKGROUND

2.1 Statistical Capacitance Extraction

Random variations are usually modeled with a set of random variables ξ. For interconnect capacitance extraction, we restrict the random variables to the geometric parameters of conductor. Their variation behavior is often assumed to follow the spatially correlated multivariate Gaussian distribution:

$$\rho(\xi_i) = \frac{1}{\sqrt{2\pi}\sigma} \exp(-\frac{\xi_i^2}{2\sigma^2}) \quad , \tag{1}$$

$$\text{cov}(\xi_i, \xi_j) = \sigma^2 \exp(\frac{-|\vec{r}_i - \vec{r}_j|^2}{\eta^2}) \quad . \tag{2}$$

where $\rho(\xi_i)$ is the possibility density function (PDF) of the i'th variable ξ_i, and σ is the standard derivation (Std). The spatial correlation between two variables are reflected by the correlation function in (2), where η is called correlation length. $\vec{r}_i$ and $\vec{r}_j$ are the spatial positions associated with ξ_i and ξ_j, respectively. There are other forms of correlation function, which may be extracted through sophisticated techniques using statistical data from actual chips [1]. The larger the correlation length, the stronger the correlation between variables spatially close to each other is.

The boundary element method (BEM) is one of the main 3-D capacitance extraction approaches for deterministic interconnect structures. The surfaces of conductor are firstly dissected into 2-D panels, for each of which a uniform charge distribution is assumed. With the potential at a panel center expressed as the sum of contributions from all panel charges, a linear equation system is formed [5-7]:

$$\boldsymbol{Pq} = \boldsymbol{v} \quad . \tag{3}$$

Here $\boldsymbol{P}$ is called potential coefficient matrix; $\boldsymbol{v}$ consists of the voltages imposed on the conductors; $\boldsymbol{q}$ is the unknown vector of panel charges. The capacitances are computed by summing up the panel charges on each conductor.

The main object of accurate statistical capacitance extraction is to obtain a high-order capacitance representation with respect to a set of random variables. A second order (quadratic) representation is sufficient in most applications [8]. For this purpose, the methods in [5, 7] firstly expand the matrix entry of $\boldsymbol{P}$ with a second-order form of the variables ξ, like

$$\tilde{P}_{ij} = P_{ij} + \tilde{\boldsymbol{a}}_{ij}^T \boldsymbol{\xi} + \boldsymbol{\xi}^T \tilde{A}_{ij} \boldsymbol{\xi} \quad . \tag{4}$$

Then, after matrix conversion, the statistical charge vector $\tilde{\boldsymbol{q}}$ and further capacitance, can be obtained. The perturbation method includes invoking d^2 times of deterministic capacitance extraction for the quadratic model, where d is the number of independent variables. This method may have large error [6] [1], partially because high-order items are truncated at the both stages of forming $\tilde{\boldsymbol{P}}$ and solving for $\tilde{\boldsymbol{q}}$. The Hermite polynomial chaos method used in [6, 9] has the same order of complexity but higher accuracy, and is introduced in the following subsection.

2.2 Hermite Polynomial Chaos Techniques

Essentially, the HPC method in [9] is the same as the SSCM of [6]. Ref. [9] gives a concise presentation of it and points out a distinct advantage that the method can suit to any deterministic capacitance solver, even formula-based capacitance solver. Below the main techniques in [6] and [9] are briefly introduced.

The statistical capacitance $\tilde{C}$ can be expressed with the Hermite polynomial expansion:

$$\tilde{C}(\boldsymbol{\zeta}) = a_0 \Psi^0 + \sum_{i_1=1}^{d} a_{i_1} \Psi^1(\zeta_{i_1}) + \sum_{i_1=1}^{d}\sum_{i_2=1}^{i_1} a_{i_1 i_2} \Psi^2(\zeta_{i_1}, \zeta_{i_2}) + \cdots \tag{5}$$

where $\boldsymbol{\zeta} = (\zeta_1, \ldots, \zeta_d)$ is a set of independent Gaussian random variables, and Ψ^i are the Hermite polynomials of the i'th order. Specifically, the Hermite polynomials below order 3 are:

$$\Psi^0 = 1, \quad \Psi^1(\zeta_i) = \zeta_i, \quad \Psi^2(\zeta_i, \zeta_j) = \zeta_i \zeta_j - \delta_{ij} \quad , \tag{6}$$

where δ_{ij} is the Kronecker delta function. The Hermite polynomial expansion is guaranteed to converge for any Gaussian random process with finite second-order moments [11]. Moreover, the Askey principle [12] shows that the expansion has the optimal convergence rate.

The Hermite polynomials can further be labeled consistently to simplify (5):

$$\tilde{C}(\boldsymbol{\zeta}) = \sum_{j=1}^{\infty} \tilde{c}_j \Psi_j(\boldsymbol{\zeta}) \quad , \tag{7}$$

where Ψ_j is the j'th Hermite polynomials in ascending order. The Hermite polynomials satisfy the following orthogonal property:

$$< \Psi_j(\boldsymbol{\zeta}), \Psi_k(\boldsymbol{\zeta}) >_\rho = \alpha_j \delta_{jk}, \quad \alpha_j > 0 \tag{8}$$

where α_j are constant values, and the subscript ρ means that the variables obey the Gaussian distribution. The inner product in (8) is defined as the mathematical expectation of the product of the two stochastic functions:

$$< X, Y >_\rho = E(XY) \quad . \tag{9}$$

For quadratic capacitance model, the terms with order larger than 2 in (7) are truncated. This approximation of capacitance is denoted by $C(\boldsymbol{\zeta})$:

$$C(\boldsymbol{\zeta}) = \sum_{j=1}^{M} c_j \Psi_j(\boldsymbol{\zeta}) \quad , \tag{10}$$

where M is the number of Hermite polynomials, $M = d^2/2 + 3d/2 + 1$. The coefficients can be evaluated with:

$$c_j = \frac{1}{\alpha_j} < C(\boldsymbol{\zeta}), \Psi_j(\boldsymbol{\zeta}) >_\rho \quad , j=1, \ldots, M \quad . \tag{11}$$

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[1] Experiment results in [5] even show a probability density function of capacitance with both positive and negative values.

According to (9), we need to compute a d-dimensional integral:

$$< C(\zeta), \Psi_j(\zeta) >_\rho = \int C(\zeta) \Psi_j(\zeta) \rho(\zeta) d\zeta \quad . \qquad (12)$$

The Gaussian-Hermite quadrature technique can be used, which has a form of weighted summation:

$$< C(\zeta), \Psi_j(\zeta) >_\rho = \sum_{i=1}^{N} w_i C(\zeta^i) \Psi_j(\zeta^i) \quad , \qquad (13)$$

where ζ^i is the ith Hermite-Gaussian integral point. Therefore, the variational capacitance model can be obtained after solving N deterministic structures defined by the geometric parameters ζ^i.

To improve the computational efficiency, the number of integral points N in (13) can be further reduced with the sparse grid quadrature [13]. It is proved in [9], that level-2 sparse grid is required for the quadratic capacitance model. This makes N about $2d^2$, much less than 3^d for the case using the Gaussian-Hermite quadrature. The sparse grid based method can be accelerated also by combining coincident integral points with different weights, or adopting the technique of minimum spanning tree [6] when extracting deterministic capacitances with iterative linear equation solver.

3. CONTINUOUS SURFACE MODEL FOR GEOMETIRC VARIATIONS

3.1 Model for One-Direction Variation

The geometric variation model in [5-7] assumes each quadrilateral panel on nominal conductor surface fluctuates along the normal direction of surface separately, but keeps its shape unchanged. Thus, discontinuous conductor surfaces are generated, as that shown in Fig. 1(a). Under this model, the total area of conductor surfaces is the same as that of the nominal conductor, and the fragmented surface obviously deviates from the actual situation.
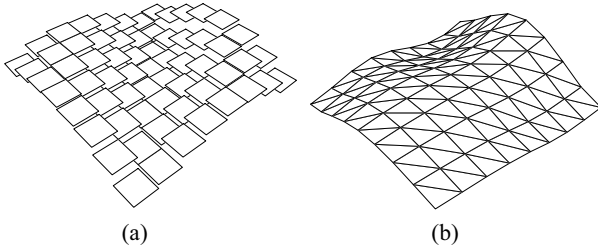

(a)   (b)

Figure 1. A variational plane generated with: (a) the model used in [5-7], (b) the continuous surface model.

A straightforward remedy to the simplified model can be made by characterizing the fluctuations of vertices of nominal panels separately. Since four vertices of a panel may not lie on a same plane, the triangular discretization is needed for the variational surface. Thus, the modified geometric variation model generates a continuous surface (as shown in Fig. 1(b)), where the random variables are imposed on the panel vertices. This variational surface model converges to a smooth shape as the triangular mesh becomes denser. The grid size of triangular mesh in practical use depends on the accuracy requirement of BEM capacitance solver and the extent of variation.

For a plane structure, the nominal vertices fluctuate along only one direction (normal to the nominal surface). Thus, one variable is associated with one nominal vertex, as one variable corresponds to one nominal panel in the simplified model. Since the number of vertices is about half of the number of panels for the triangular

discretization, the number of variables will also be half of that in the simplified model if both models have same number of panels. For BEM capacitance solver, the assumption of same number of panels usually implies the comparable result accuracy.

3.2 Model for Two-Direction Variation

The above model is suitable for the cases where only one-direction variation is considered. For actual interconnect wire, modeling two-direction variations of height and width is often needed. In this case, the model for one-direction variation will encounter difficulty. Since surface fluctuation occurs along two directions, the projection of top surface on the XOY plane is different from the nominal shape. Fig. 2 shows an example of the effect of two-direction fluctuation, where the projection of arris is not a straight line. So, we do not have a certain nominal shape for the top surface and thus cannot construct the variational surface through disturbing the nominal vertices.
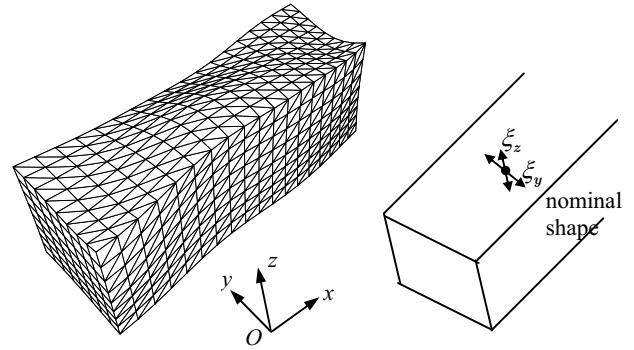

Figure 2. A metal wire with two-direction fluctuation, and the illustration of nominal shape with two-direction variables.

To model the two-direction variation, we extend the one-direction model by defining two variables for each discretization vertex on the nominal conductor. For each vertex on a wire routed along X-axis, random variables ξ_z and ξ_y are defined to represent the fluctuations along Z-axis and Y-axis, respectively (see Fig. 2). The variables for two directions form two variable sets, each of which obeys a Gaussian distribution with spatial correlation. With this model, the continuous variational surface can be easily generated. Now the number of variables approximates the number of triangular panels. So, if the continuous model employs the same number of panels as the simplified model, the number of variables will not increase.

3.3 Comparison Results

In this subsection, we compare the continuous surface model and simplified model in [5-7], through Monte Carlo (MC) simulations. For various discretization density, the MC simulation with 10000 samples is performed; the capacitances of each sample structure are extracted with FastCap 2.0 [14].

The first structure is a 1μm×1μm plane. The densest discretization mesh includes 800 panels, whose result is regarded as golden value. The simulation results for two variation models are listed in Table 1. Experimental results on the corresponding non-variation plane show that the capacitance error is less than 1% if the panel number is not less than 242. Table 1 shows that the variational capacitance with the continuous surface model has the same convergence property. But with the simplified model, a

comparable panel number corresponds to a nearly 8% error of capacitance Std. With denser discretization, simulation results show the simplified model still results in large error of Std.

Table 1. Simulation results for the plane (σ=0.2μm, η=1μm)

	Continuous surface model			Simplified model	
Num. of panel	800	242	392	256	400
Mean (10^{-18}F)	41.656	41.235	41.427	41.224	41.411
Std (10^{-18}F)	0.854	0.840	0.854	0.788	0.793
Err. of Mean	--	-1.0%	-0.5%	-1.0%	-0.6%
Err. of Std	--	-1.6%	0.0%	**-7.7%**	**-7.1%**

The second structure includes two parallel wires (2-bit bus). The width, height and length of each wire are 1μm, 1μm and 4μm, respectively. The wire spacing is 2μm. The width and height variations are assumed to have same Std and correlation length. The simulation errors of both models for different discretization are listed in Table 2, where the results for 4096-panel discretization are regarded as golden value. From Table 2, we can see that the Std error of total capacitance C_{11} from the simplified model is prominent, just as the simulation results for plane structure.

Table 2. Simulation results for the 2-bit bus (σ=0.2μm, η=8μm)

		Continuous surface model		Simplified model	
Num. of panel		4096	640	1536	640	1568
Err. of C_{11}	Mean	--	-1.5%	-0.6%	-1.1%	-0.4%
	Std	--	0.3%	1.4%	**-6.7%**	**-5.0%**
Err. of C_{12}	Mean	--	2.2%	0.8%	1.7%	0.6%
	Std	--	-1.2%	1.0%	-1.1%	-0.5%

Due to variables of both side surfaces are correlated, and the wire width is the difference of two $N(0, \sigma^2)$ distribution, the Std of width in this case is actually $\sqrt{2\sigma^2(1-\exp(-1/64))}$ =0.035μm. The Std of height is the same small quantity. For larger variance of width and height, the error of simplified model would be larger.

4. VARIATION-AWARE EXTRACTION CONSIDERING WINDOW TECHNIQUE

In this section, the chip-level capacitance extraction in [9] is extended to consider the continuous surface model for geometric variations. For chip-level extraction, the window technique is necessary to limit the problem size. Only the small structures within windows are simulated with a BEM solver. Then, the capacitance elements from different windows form a distributed circuit for further analysis, or are used to assemble the total and coupling capacitances of whole critical net. Sophisticated techniques for window partition and assembling can be employed to guarantee high accuracy [15].

With consideration of window technique, the main tasks for variational capacitance extraction include the intra-window extraction, and the calculation of capacitance covariance between windows [9]. Because the continuous surface model involves much larger number of random variables than [9], efficient variable reduction is needed for the intra-window extraction. Since different windows are associated with each other through the physical variables, not the variables in capacitance model, calculating the capacitance covariance becomes an issue.

4.1 Intra-Window Extraction and Variable Reduction with Weighted PFA

For intra-window structure, we employ the techniques in Section 2.2 to obtain the quadratic capacitance expression (10). The computational time is proportional to d^2, where d is the number of independent variables. Random variable reduction must be performed for the proposed geometric variation model.

The principle factor analysis (PFA) is employed in [5-7] to reduce the random variables, which is done by eigen-decomposition on the covariance matrix $\Delta n(\xi)$ of geometric random variables ξ. If the first K largest eigenvalues are $\lambda_1, \lambda_2, \ldots, \lambda_K$, and $e_1, e_2, \ldots, e_K$ are the corresponding eigenvectors, the variables ξ can be approximated by the linear combination of K dominant variables ζ [5-7]:

$$\xi \approx \sum_{i=1}^{K} \sqrt{\lambda_i} e_i \zeta_i \qquad . \tag{14}$$

Here $\{\zeta_i\}$ is a set of independent variables with $N(0,1)$ distribution, that can be used to form the Hermite polynomial chaos (10). Thus, the intra-window extraction includes the following main steps:

1). Perform the eigen-decomposition for the covariance matrix of physical variations generated by (2) to obtain the first K largest eigenvalues and eigenvectors.

2). With the technique of sparse grid quadrature, obtain the integral points ζ^i and corresponding weights.

3). For each ζ^i, convert it to physical parameters ξ^i with (14), and then generate and extract the deterministic conductor structure with continuous surfaces. This step obtains the deterministic capacitances $C(\zeta^i)$.

4). Calculate the coefficients of the quadratic capacitance expression with (11) and (13).

It should be addressed that the number of dominant variables required in PFA mainly depends on the correlation function (2) and is independent of the BEM discretization. Another comment is that, the eigen-decomposition is not very time-consuming, since it is performed only once and the dimension of covariance matrix for intra-window structure is just moderate. If there are several groups of variables and no correlation between any two groups, the PFA shall be performed for each group separately.

The PFA method compares variable parameters one with another without considering their different impact on the output capacitance. A new variable reduction technique was proposed in [16] to take the impact on output performance into account. Inspired by [16], we propose a weighted PFA (wPFA) technique for better variable reduction.

If a weight is defined for each physical variable ξ_i to reflect its impact on output, then a set of new variables ξ^* are formed:

$$\xi^* = W\xi \quad , \tag{15}$$

where W is a diagonal matrix of weights. The covariance matrix $\Delta n(\xi^*)$ of ξ^* includes the weight information, and performing PFA based on it makes weighted variable reduction. We have

$$\Delta n(\xi^*) = E(W\xi(W\xi)^T) = W\Delta n(\xi)W^T \quad , \tag{16}$$

and denote its eigenvalues and eigenvectors by $\{\lambda_i^*\}$ and $\{e_i^*\}$. Then, the variables ξ can be approximated by the linear combination of a set of independent dominant variables ζ^*:

$$\xi = W^{-1}\xi^* \approx W^{-1}\sum_{i=1}^{K}\sqrt{\lambda_i^*}e_i^*\zeta_i^* \quad . \tag{17}$$

For capacitance extraction, the capacitance value is the sum of panel charges, and the charge distribution is not uniform. At

different positions, there is charge contribution with different significance. Based on this observation, we define the weight for variable ξ_i according to the charge density around its position. Firstly we perform capacitance extraction on the nominal structure to get a charge distribution. Then, the charge density of panel is reassigned to its vertices. The charge density $q_{v,i}$ for vertex i is:

$$q_{v,i} = \sum_{\vec{r}_i \in panel_j} \frac{q_j}{3S_j} \quad , \tag{18}$$

where q_j and S_j are the charge and area of panel j, respectively. $\vec{r}_i$ stands for the vertex corresponding to variable ξ_i. Finally, the weight is calculated as the square ratio of vertex charge density to its minimum value:

$$w_i = \frac{q_{v,i}^2}{\min_i(q_{v,i}^2)} \quad . \tag{19}$$

The matrix W is formed with w_i as diagonal entries. Except one additional extraction of nominal structure, the weighted PFA hardly increases computational expense of PFA as W is diagonal.

4.2 Inter-Window Covariance of Capacitance

Because the variable parameters belonging to different windows may be correlated, the corresponding capacitances from these windows have nonzero covariance [9]. After intra-window extraction, we suppose the quadratic capacitance expressions for the kth capacitance in windows i and j are

$$C_{i,k} = \sum_{p=1}^{M_i} c_{i,k,p} \Psi_p(\boldsymbol{\zeta}^*) \quad \text{and} \quad C_{j,k} = \sum_{p=1}^{M_j} c_{j,k,p} \Psi_p(\boldsymbol{\zeta}'^*) \ ,$$

respectively. The covariance of capacitance can be evaluated with:

$$\text{cov}(C_{i,k}, \ C_{j,k}) = \sum_{p=1}^{M_i}\sum_{q=1}^{M_j} c_{i,k,p} c_{j,k,q} \, \text{cov}(\Psi_p(\boldsymbol{\zeta}^*), \Psi_q(\boldsymbol{\zeta}'^*)). \tag{20}$$

Here $\boldsymbol{\zeta}^*$ and $\boldsymbol{\zeta}'^*$ are dominant variable sets in windows i and j, respectively. Thus, the problem becomes calculating the covariance between Hermite polynomials.

We first determine the covariance between a variable ζ_a^* in windows i and a variable $\zeta_b'^*$ in windows j. The relationship between $\boldsymbol{\zeta}^*$ and physical variables $\boldsymbol{\xi}$ in the weighted PFA (17) can be rewritten as

$$\boldsymbol{\xi} = \boldsymbol{L}_i \boldsymbol{\zeta}^* \ , \tag{21}$$

where $\boldsymbol{L}_i$ is a $n \times K$ matrix. n is the number of correlated physical variables, and K is the number of dominant factors. With the concept of pseudo inverse, we derive from (21):

$$\boldsymbol{\zeta}^* \approx \boldsymbol{G}_i \boldsymbol{\xi} \ ,$$

where $\boldsymbol{G}_i$ is the pseudo inverse of $\boldsymbol{L}_i$, with dimensions of $K \times n$:

$$\boldsymbol{G}_i = (\boldsymbol{L}_i^T \boldsymbol{L}_i)^{-1} \boldsymbol{L}_i^T \quad . \tag{22}$$

Now,

$$\begin{aligned}\text{cov}(\zeta_a^*, \zeta_b'^*) &= \text{cov}(\sum_s g_{i,a,s}\xi_s, \ \sum_r g_{j,b,t}\xi_t') \\ &= \sum_s\sum_t g_{i,a,s} g_{j,b,t} \, \text{cov}(\xi_s, \xi_t')\end{aligned} \tag{23}$$

where $g_{i,a,s}$ and $g_{j,b,t}$ represent matrix entries of $\boldsymbol{G}_i$ and $\boldsymbol{G}_j$, respectively. $\text{cov}(\xi_s, \xi_t')$ can be checked out from the geometric variation model.

With the covariance between two dominant variables from

different windows, we can calculate the covariance between Hermite polynomials as in [9]. For problem with large n, directly calculating (23) is time-consuming. Considering the attenuation of correlation function (2), we can ignore the covariance item of two variables physically far away from each other. This will reduce the expense of calculating (23).

The inter-window covariance of capacitance can be used to calculate the full-path capacitance. The mean values of relevant intra-window capacitances are assembled to obtain the mean of full-path capacitance, with the same manner as non-statistical extraction [15]. If considering a simple window technique with windows non-overlapping, the capacitance variance (the square of Std) of a whole net k can be calculated with [9]:

$$D(C_k) = D(\sum C_{ki}) = \sum_i D(C_{ki}) + 2\sum_{i \neq j} \text{cov}(C_{ki}, C_{kj}) \ , \tag{24}$$

where C_{ki} stands for the related window capacitance, whose summation approximates the capacitance C_k for net k. The technique to obtain the PDF of capacitance is also available in [9].

5. NUMERICAL RESULTS

The proposed techniques are implemented with MATLAB, which generates the deterministic sample structures and calculates the statistical capacitances. The sample structures are extracted with FastCap 2.0 [14]. For comparison, the MC simulation with 10000 samples is also performed. For each test case, the continuous geometric model with two-direction variation is assumed. Since the rough-surface effect is not prominent for on-chip interconnects, we set the correlation lengths to be 8 to 9 times of conductor width, like [6]. All experiments are carried out on a Linux server with 8 Xeon CPUs with 2.33GHz.

5.1 Small Cases

Two small structures are firstly tested. They are 2-bit bus and 1×1 crossover. The width, height and length of each wire are 1μm, 1μm and 4μm, respectively. The spacing of wires is 1μm, the same for two cases. Each case includes 768 triangular panels. The techniques of HPC and that in Section 4.1 are used to calculate the statistical capacitances. For both PFA and wPFA, the truncation criterion of eigenvalues is 0.1%.

For the 2-bit bus structure, the correlation lengths for height variation and width variation are 8μm and 9μm respectively. The variation Std's for the two directions are 0.15μm and 0.2μm. Their computational results are listed in Table 3, along with the error to the results of MC simulation. The table shows that both HPC techniques have good accuracy. For this case, wPFA reduces the number of variables to 9, instead of 11 by PFA. The integral points for sparse-grid quadrature are reduce from 276 to 191 (**30% reduction**). The speedup of HPC with wPFA to 10000-times MC simulation is about $10000/191 \approx 52$.

Table 3. Results for the 2-bit bus (in unit of 10^{-18}F)

		MC	HPC(PFA)	Error	HPC(wPFA)	Error
C_{11}	Mean	172.0	172.0	0.0%	172.0	0.0%
	Std	1.640	1.609	-1.9%	1.614	-1.6%
C_{12}	Mean	-82.4	-82.3	0.1%	-82.4	0.0%
	Std	1.720	1.799	4.6%	1.770	3.0%

For the 1×1 crossover structure, the computational results are listed in Table 4. The settings of correlation length and variation Std are the same as those for the 2-bit bus. Table 4 also shows the accuracy of proposed techniques. For this case, wPFA reduces the number of variables to 9, instead of 12 by PFA. The integral

points are reduced by **41%** with wPFA. The speedup of HPC with wPFA to 10000-times MC simulation is about **52**.

Table 4. Results for the 1×1 crossover (in unit of 10^{-18}F)

		MC	HPC(PFA)	Error	HPC(wPFA)	Error
C_{11}	Mean	169.0	169.0	0.0%	169.0	0.0%
	Std	1.808	1.738	-3.9%	1.783	-1.4%
C_{12}	Mean	-81.1	-81.3	-0.2%	-81.2	-0.1%
	Std	1.727	1.774	2.7%	1.746	1.1%

5.2 A Large Case for Full-Path Extraction

The experiment for a large structure is carried out to validate the accuracy and efficiency of the techniques presented in Section 4.2. This case contains two parallel lines dissected into 10 windows, and parameter settings are just the same as the first case in [9]. The sample geometry of this case is constructed with the continuous surface model, rather than the grid-based simple model assumed by [9]. According to the correlated multivariate Gaussian distribution, 10000 sample structures are generated. For each one, the structure is divided into 10 windows for extraction and the capacitance results of all windows are summed up to obtain the full-path capacitances. The results for 10000 samples are then collected to get the MC simulation results. While using the proposed techniques, we extract the statistical capacitance expressions for each window separately. Then, the statistical full-path capacitances are calculated with the techniques proposed in Section 4.2. The comparison of full-path capacitances are shown in Table 5.

Table 5. Results of the full-path capacitances (in unit of 10^{-18}F)

		MC	HPC(wPFA)	Error
C_{11}	Mean	1483	1484	0.1%
	Std	8.76	8.87	1.3%
C_{12}	Mean	-511	-513	-0.4%
	Std	6.68	7.34	9.8%

From Table 5, we can see the results of proposed techniques match those from 10000-times MC simulation. This validates the accuracy of the techniques in Section 4.2. It is also found out that the mean of C_{11} has little discrepancy with that in [9], but the Std of C_{11} is much less than the latter (see Fig. 4(a) of [9]). Because [9] is based on an over-simplified model, its results obviously largely overestimate the capacitance variation.

For this case, each window includes 1024 triangular panels, and the wPFA reduces the variables to 8 dominant factors. The HPC solves 154 deterministic structures for each window. The speedup to 10000-times MC is expected to be $10000/154 \approx$ **64**. The actual breakdown of computational times is listed in Table 6. From the table we see that additional 40.5 seconds are spent on calculating the statistical full-path capacitance, mainly devoted to calculating the capacitance variance with (23) and (24). And, the actual speedup to MC simulation is still as large as **58**.

Table 6. CPU time (in second) of the full-path extraction

MC	Proposed method			Speedup
	HPC(wPFA)	Full-path variances	Total	ratio
20918	322	40.5	362.5	58

6. CONCLUSIONS

The main contributions of this work are as follows:

1) A continuous surface model is proposed for the geometric variations of on-chip interconnects. Compared with the currently used model, the new model does not increase number of variables and guarantees accurate modeling of capacitance variance.

2) Based on the continuous surface model, efficient techniques for chip-level extraction of variational capacitance are presented, including the HPC technique for intra-window extraction and the calculation of inter-window capacitance covariance.

3) A weighted PFA technique for capacitance extraction is proposed to reduce the random variables. Its advantages over the original PFA are preliminarily demonstrated by experiments.

7. ACKNOWLEDGEMENT

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